CLAIMS

What is claimed is.

1	1. A phase-change memory device comprising:		
2	spaced-apart first and third active areas that are disposed in a substrate;		
3	a recess comprising a bottom and walls, wherein the recess communicates to the		
4	first active area and the third active area; and		
5	a polysilicon film disposed in the recess, wherein the polysilicon film has a first		
3	conductivity at the bottom and a second conductivity at the walls.		
1	2. The phase-change memory device according to claim 1, wherein the first and		
2	second active areas are spaced apart along a first symmetry line, further comprising:		
3	a third active area that is spaced apart from the first active area along a second		
4	symmetry line that is orthogonal to the first symmetry line, wherein the polysilicon film		
5	is continuous between the first active area and the second active area.		
1	3. The phase-change memory device according to claim 1, wherein the first and		
2	third active areas are spaced apart along a second symmetry line, further comprising:		
3	a second active area that is spaced apart from the first active area along a first symmetry		
4	line that is orthogonal to the second symmetry line.		
1	4. The phase-change memory device according to claim 1, further comprising:		
2	a first isolation structure that is disposed in the substrate parallel to the second		
3	symmetry line.		

1	5.	The phase-change memory device according to claim 1, further comprising:
2		a first isolation structure that is disposed in the substrate parallel to the second
3	symm	etry line; and
4		a second isolation structure that is disposed in the substrate orthogonal to the first
5	isolati	on structure.
1	6.	The phase-change memory device according to claim 1, further comprising:
2		a first isolation structure that is disposed in the substrate parallel to the second
3	symm	etry line; and
5	Symm	ony mo, and
4		a second isolation structure that is disposed in the substrate orthogonal to the first
5	isolati	on structure, and wherein the first isolation structure comprises a discontinuous
6	upper	surface and the second isolation structure comprises a substantially continuous
7	upper	surface.
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1	7.	The phase-change memory device according to claim 1, wherein the first active
2	area comprise	es a memory cell structure comprising:
3		a P+ Si structure disposed upon an N Si structure, wherein the P+ Si structure has
4	a top	and a bottom, wherein the N Si structure has a top and a bottom; and wherein the
5	secon	d isolation structure has a top and a bottom; and

wherein the second isolation structure bottom is below the P+ Si structure.

1 8. The phase-change memory device according to claim 1, wherein the first active 2 area comprises a memory cell structure comprising:

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a P+ Si structure disposed upon an N Si structure, wherein the P+ Si structure has a top and a bottom, wherein the N Si structure has a top and a bottom; and wherein the second isolation structure has a top and a bottom; and

wherein the second isolation trench bottom is below the P+ Si structure, and wherein the second isolation structure top is above the P+ Si structure bottom.

2	in a substrate, a trench that exposes first, and second active areas along a first
3	symmetry line and that exposes the first and a third active area along a second symmetry
4	line that is orthogonal to the first symmetry line;
5	a polysilicon film disposed in the trench, wherein the polysilicon film contacts the
6	first and third active areas; and
7	a phase-change memory element disposed above the first active area.
1	10. The memory device according to claim 9, further comprising:
2	a fourth active area;
3	and wherein the polysilicon film further comprises:
4	a first polysilicon film portion that is disposed between the first and third
5	active areas; and
6	a second polysilicon film portion that is disposed between the second and
7	fourth active areas.
1	11. The memory device according to claim 9, wherein the polysilicon film has a first
2	conductivity between the first active area and the third active area, and a second conductivity
3	superadjacent each active area.
1	12. The memory device according to claim 9, wherein the polysilicon film has a first
2	conductivity between the first active area and the third active area, a second conductivity

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A memory device comprising:

- 3 superadjacent each active area, and the first conductivity between the first active area and the
- 4 second active area.
- 1 13. The phase-change memory device according to claim 9, further comprising:
- a first isolation structure that is disposed in the substrate parallel to the second
- 3 symmetry line; and
- a second isolation structure that is disposed in the substrate orthogonal to the first
- 5 isolation structure.

1	14.	A process of forming a phase-change memory device comprising:
2		forming a recess in a substrate, wherein the recess exposes spaced-apart first and
3	third a	ctive areas, and wherein the recess comprises a bottom and walls;
4		forming a polysilicon film in the recess; and
5		treating the polysilicon film to have a first conductivity at the bottom and a
6	second	conductivity at the walls.
1	15.	The process according to claim 14, wherein treating comprises:
2		first angled doping the polysilicon film that is in contact with the first active area;
3	and	
4		second angled doping the polysilicon film that is in contact with the second active
5	area.	
1	16.	The process according to claim 14, wherein treating further comprises doping the
2	polysilicon fil	m to form discrete isolated regions of the second conductivity.
1	17.	The process according to claim 14, before treating, further comprising:
2		forming a temporary material in the recess; and
3		patterning the temporary material to expose the polysilicon film that is directly
4	above	the active areas.
1	18.	The process according to claim 14, before treating, further comprising:

2	forming a temporary material in the recess;	
3	patterning a mask over the temporary material; and	
4	removing a portion of the temporary material to expose the polysilicon film that is	
5	directly above the active areas.	
1	19. The process according to claim 14, further comprising:	
2	forming a first isolation trench in the substrate to define spaced-apart first and	
3	second areas; and	
4	forming a second isolation trench adjacent the first and second areas to define a	
5	third area.	
1	20. The process according to claim 19, further comprising:	
2	treating the first and third areas to form the first and third active areas.	
1	21. The process according to claim 19, wherein the second isolation trench is	
2	orthogonal to the first isolation trench.	
1	22. The process according to claim 19, wherein the second isolation trench is	
2	shallower than the first isolation trench.	

1	23.	The process according to claim 19, after forming the first isolation trench,
2	further comp	rising:
3		filling the first isolation trench with an isolation dielectric; and
4	plana	rizing the substrate.
1	24.	The process according to claim 19, after forming the first isolation trench,
2	further comp	rising:
3		forming a thermal dielectric film in the first isolation trench;
4		filling the first isolation trench with an isolation dielectric; and
5	planarizing th	ne substrate.
1	25.	The process according to claim 19, after forming the second isolation trench,
2	further comp	rising:
3		filling the second isolation trench with an isolation dielectric; and
4		planarizing the substrate.
1	26.	The process according to claim 19, after forming the second trench, further
2	comprising:	
3		forming a thermal dielectric film in the second isolation trench;
4		filling the second isolation trench with an isolation dielectric; and
5		planarizing the substrate.
1	27.	The process according to claim 19, further comprising:
2		forming a diode stack that is contiguous to the first isolation trench and the
3	secon	d isolation trench;

- filling the first isolation trench and the second isolation trench; and
- forming a self-aligned silicide layer upon the diode stack.

1	28. A process comprising:
2	forming a trench in a semiconductor substrate, wherein the trench exposes two
3	active areas that are situated along the transverse axis of the trench, and wherein the
4	trench exposes at least two active areas that are situated along the longitudinal axis of the
5	trench; and
6	forming a phase-change memory element above each active area.
1	29. The process according to claim 28, further comprising:
2	forming a polysilicon film in the recess; and
3	treating the polysilicon film to have a first conductivity at the bottom and a
4	second conductivity at the walls.
1	30. The process according to claim 28, wherein treating comprises:
2	first angled doping the polysilicon film that is in contact with the first active area;
3	and
4	second angled doping the polysilicon film that is in contact with the second active
5	area.
1	31. The process according to claim 28, wherein treating further comprises doping the
2	polysilicon film to form discrete isolated regions of the second conductivity.

The process according to claim 28, before treating, further comprising:

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patterning the temporary material to expose the polysilicon film that is dire	ectly above the
active areas.	
33. The process according to claim 28, before treating, further compris	sing:
forming a temporary material in the recess;	
patterning a mask over the temporary material; and	
removing a portion of the temporary material to expose the polysil	icon film that is
directly above the active areas.	
34. The process according to claim 28, further comprising:	
forming a polysilicon film in the recess; and	
treating the polysilicon film to have a first conductivity at the botto	om and a
second conductivity at the walls;	
planarizing the substrate to form electrode material;	
modifying a portion of the electrode material so that the electrode material	l comprises a
first portion having a first thermal coefficient of resistivity and a second portion h	aving a
	forming a temporary material in the recess; patterning a mask over the temporary material; and removing a portion of the temporary material to expose the polysil directly above the active areas. 34. The process according to claim 28, further comprising: forming a polysilicon film in the recess; and treating the polysilicon film to have a first conductivity at the botto second conductivity at the walls; planarizing the substrate to form electrode material; modifying a portion of the electrode material so that the electrode material

different second thermal coefficient of resistivity.